Reg.No.:												

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 50035

B.E. / B.Tech. DEGREE END-SEMESTER EXAMINATIONS – JAN. 2025
Fourth Semester
Computer Science and Engineering
U19CS410 - COMPUTER ORGANIZATION
(Regulation 2019)

Time: Three Hours Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	Give the significance of program counter.	2	K1	CO1
2.	Define Processor clock and clock rate.	2	K1	CO1
3.	State the various design methods of hardwired control unit.	2	K2	CO2
4.	List the address-sequencing capabilities required in a control memory.	2	K1	CO2
5.	What is data hazard in pipelining?	2	K2	CO3
6.	In a pipelined machine, the clock skew adds 5ns of overhead to each execution stage. What is the length of the pipelined stage?	2	K3	CO3
7.	List the memory hierarchy with respect to size, cost and speed.	2	K1	CO4
8.	The application program in a computer system with cache uses 1400 instruction acquisition bus cycle from cache memory and 100 from main memory. What is the hit rate?	2	K2	CO4
9.	What is the use of serial port?	2	K1	CO5
10.	Define programmed I/O.	2	K2	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.			Questions	Marks	KL	CO
11.	a)	i.	Explain in detail about the various addressing modes with example.	8	K2	CO1
		ii.	Write the basic performance equation and using this equation explain how the performance of a system can be improved.	5		
			(OR)			
	b)		Explain the addressing modes for the modern processors, and how the Effective address or Offset is determined by adding any combination of three address elements.	13	K2	CO1
12.	a)		Sketch and explain the multiple bus organization in detail. Highlight the benefits of using Multiple-Bus Architecture compared to Single-Bus Architecture?	13	K2	CO2
			(OR)			
	b)	i.	What is an Instruction Cycle? Explain the 6 steps of instruction execution by CPU.	6	K2	CO2
		ii.	Enunciate on Nano Programming. Why is Nano programming essential in current day systems?	7	K2	
13.	a)		The time delay for 4 segments in pipeline are as follows: t1=50ns, t2=30ns, t3=95ns and t4=45ns. The interface register delay time tr=5ns. How long would it take to add 100 pairs of numbers in the pipeline and how can we reduce the total time to about one half of the time calculated.	13	K4	CO3
			(OR)			
	b)		Elucidate Instruction Hazards which causes to stall and illustrate how the performance of the instruction pipeline can be improved.	13	K4	CO3
14.	a)		Examine the cache memory organization and the various techniques for improving cache performance in detail.	13	K3	CO4
			(OR)			
	b)		Sketch and explain the various types of secondary storage devices.	13	K2	CO4
15.	a)		Explain the DMA with bus arbitration and its types in detail.	13	K2	CO5
			(OR)			
	b)	i.	Explain the Architecture of PCI & SCSI with diagram.	10	K2	CO5
		ii.	Write down the functions of input-output interface.	3	K2	

PART – C

(1 x 15 = 15Marks)

Q.No.		Questions	Marks	KL	CO
16. a)	i.	Explain the control sequence for execution of given instruction Add (R3), R1.	8	K3	CO2
	ii.	Illustrate control sequence for an unconditional branch instruction with example.	7		
		(OR)			
b)		In a k-way set associative cache, the cache is divided into v sets, each of which consists of k lines. The lines of a set placed in sequence one after another. The lines in set s are sequenced before the lines in set (s+1). The main memory blocks are numbered 0 onwards. The main memory block numbered 'j' must be mapped to any one of the following cache lines. Justify the answer. 1. (j mod v) x k to (j mod v) x k + (k-1) 2. (j mod v) to (j mod v) + (k-1) 3. (j mod k) to (j mod k) + (v-1) 4. (j mod k) x v to (j mod k) x v + (v-1)	15	K5	CO4